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1 New perspectives in physical design: Uncertainty-aware circuit optimization

Xiaoliang Bai, Chandu Visweswariah, Philip N. Strenski

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(131.43 KB) Additional Information: full citation, abstract, references, citings, index terms

Almost by definition, well-tuned digital circuits have a large number of equally critical paths, which form a so-called "wall" in the slack histogram. However, by the time the design has been through manufacturing, many uncertainties cause these carefully aligned delays to spread out. Inaccuracies in parasitic predictions, clock slew, model-to-hardware correlation, static timing assumptions and manufacturing variations all cause the performance to vary from prediction. Simple statistical princip ...

Keywords: circuit tuning, nonlinear, optimization, performance optimization, process variation, small uncertainty, transistor sizing

2 Block-based Static Timing Analysis with Uncertainty

Anirudh Devgan, Chandramouli Kashyap

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(181.39 KB) Additional Information: full citation, abstract, index terms

Static timing analysis is a critical step in design of any digitalintegrated circuit. Technology and design trends have ledto significant increase in environmental and process variationswhich need to be incorporated in static timing analysis.This paper presents a new, efficient and accurate block-basedstatic timing analysis technique considering uncertainty.This new method is more efficient as its modelsarrival times as cumulative density functions (CDFs) anddelays as probability functions (PDFs ...

3 Design automation methodology and rf/analog modeling for rf CMOS and SiGe BiCMOS technologies

D. L. Harame, K. M. Newton, R. Singh, S. L. Sweeney, S. E. Strang, J. B. Johnson, S. M. Parker, C. E. Dickey, M. Erturk, G. J. Schulberg, D. L. Jordan, D. C. Sheridan, M. P. Keene, J. Boquet, R. A. Groves, M. Kumar, D. A. Herman, B. S. Meyerson

March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

Additional Information: full citation, abstract, references, index terms

The rapidly expanding telecommunications market has led to a need for advanced rf

integrated circuits. Complex rf- and mixed-signal system-on-chip designs require accurate prediction early in the design schedule, and time-to-market pressures dictate that design iterations be kept to a minimum. Signal integrity is seen as a key issue in typical applications, requiring very accurate interconnect transmission-line modeling and RLC extraction of parasitic effects. To enable this, IBM has in place ...

4 Low-power circuits and technology for wireless digital systems

S. V. Kosonocky, A. J. Bhavnagarwala, K. Chin, G. D. Gristede, A.-M. Haen, W. Hwang, M. B. Ketchen, S. Kim, D. R. Knebel, K. W. Warren, V. Zyuban

March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

Additional Information: full citation, abstract, references, citings, index terms

As CMOS technology scales to deep-submicron dimensions, designers face new challenges in determining the proper balance between aggressive high-performance transistors and lower-performance transistors to optimize system power and performance for a given application. Determining this balance is crucial for battery-powered handheld devices in which transistor leakage and active power limit the available system performance. This paper explores these questions and describes circuit techniques fo ...

5 Coping with variability: the end of deterministic design: Death, taxes and failing chips

Chandu Visweswariah

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(145.71 KB) Additional Information: full citation, abstract, references, citings, index terms

In the way they cope with variability, present-day methodologies are onerous, pessimistic and risky, all at the same time! Dealing with variability is an increasingly important aspect of high-performance digital integrated circuit design, and indispensable for first-time-right hardware and cutting-edge performance. This invited paper discusses the methodology, analysis, synthesis and modeling aspects of this problem. These aspects of the problem are compared and contrasted in the ASIC and custom ...

Keywords: Statistical timing, design methodology, parametric yield prediction

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("design validation" <in> ti)

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('design validation' <in> ti) Search

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---

1 **Vertical drop impact test system for biomechanical injury assessme design validation and model development**
Schmaltz, D.; Harris, G.F.; Yogananadan, N.; Pintar, F.; Sances, A., Jr.;
Engineering in Medicine and Biology Society, 1989. Images of the Twenty-Firs Century. Proceedings of the Annual International Conference of the IEEE Engineering in , 9-12 Nov. 1989
Pages:811 - 812 vol.3

[Abstract] [PDF Full-Text (80 KB)] IEEE CNF

---

2 **High speed data bus design validation**
Stevens, R.;
Aerospace and Electronics Conference, 1991. NAECON 1991., Proceedings of t IEEE 1991 National , 20-24 May 1991
Pages:197 - 201 vol.1

[Abstract] [PDF Full-Text (316 KB)] IEEE CNF

---

3 **New design error modeling and metrics for design validation**
Kang, S.; Szygenda, S.A.;
Design Automation Conference, 1992. EURO-VHDL '92, EURO-DAC '92. European , 7-10 Sept. 1992
Pages:472 - 477

[Abstract] [PDF Full-Text (460 KB)] IEEE CNF

---

4 **Automatic error pattern generation for design error detection in a d validation simulation system**
Kang, S.; Szygenda, S.A.;
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE

International , 21-25 Sept. 1992
Pages:533 - 536

[Abstract] [PDF Full-Text (332 KB)] IEEE CNF

---

5 **An intelligent network test-bed for service design, validation and execution**
Bosco, P.G.; Faraci, F.;
Digital Communications, 1992. 'Intelligent Networks and their Applications.' Proceedings., 1992 International Zurich Seminar on , 16-19 March 1992
Pages:B2/1 - B216

[Abstract] [PDF Full-Text (776 KB)] IEEE CNF

---

6 **Design validation: comparing theoretical and empirical results of de error modeling**
Sungho Kang; Szygenda, S.A.;
Design & Test of Computers, IEEE , Volume: 11 , Issue: 1 , Spring 1994
Pages:18 - 26

[Abstract] [PDF Full-Text (660 KB)] IEEE JNL

---

7 **Integrated Design/validation Methodology For Fault Tolerant (dependable) Computing Systems**
Bettencourt, C.;
Integrating Error Models with Fault Injection, 1994., Third Int'l Workshop on , 25-26, 1994
Pages:10 - 12

[Abstract] [PDF Full-Text (204 KB)] IEEE CNF

---

8 **High-level design validation using algorithmic debugging**
Naganuma, J.; Ogura, T.; Hoshino, T.;
European Design and Test Conference, 1994. EDAC, The European Conferenc Design Automation. ETC European Test Conference. EUROASIC, The Europear Event in ASIC Design, Proceedings. , 28 Feb.-3 March 1994
Pages:474 - 480

[Abstract] [PDF Full-Text (556 KB)] IEEE CNF

---

9 **Using simulation for design validation of switching power converter**
Chwirka, S.;
Circuits and Systems, 1994., Proceedings of the 37th Midwest Symposium on , Volume: 1 , 3-5 Aug. 1994
Pages:701 - 707 vol.1

[Abstract] [PDF Full-Text (380 KB)] IEEE CNF

---

10 **An optoelectric plantar "shear" sensing transducer: design, validati and preliminary subject tests**
Lebar, A.M.; Harris, G.F.; Wertsch, J.J.; Hongsheng Zhu;
Rehabilitation Engineering, IEEE Transactions on [see also IEEE Trans. on Neu Systems and Rehabilitation] , Volume: 4 , Issue: 4 , Dec. 1996

Pages:310 - 319

[Abstract] [PDF Full-Text (1324 KB)] IEEE JNL

---

11 **A unified framework for design validation and manufacturing test**
Moundanos, D.; Abraham, J.A.; Heskote, Y.V.;
Test Conference, 1996. Proceedings., International , 20-25 Oct. 1996
Pages:875 - 884

[Abstract] [PDF Full-Text (920 KB)] IEEE CNF

---

12 **ASIC design validation in a system context**
Bartlett, J.;
Verilog HDL Conference, 1996. Proceedings., 1996 IEEE International , 26-28 1996
Pages:105 - 112

[Abstract] [PDF Full-Text (788 KB)] IEEE CNF

---

13 **Rapid prototyping for communications design validation**
Courtoy, M.;
Southcon/96. Conference Record , 25-27 June 1996
Pages:49 - 54

[Abstract] [PDF Full-Text (664 KB)] IEEE CNF

---

14 **Statechart methodology for the design, validation, and synthesis of large scale asynchronous systems**
Kol, R.; Ginosar, R.; Samuel, G.;
Advanced Research in Asynchronous Circuits and Systems, 1996. Proceedings Second International Symposium on , 18-21 March 1996
Pages:164 - 174

[Abstract] [PDF Full-Text (792 KB)] IEEE CNF

---

15 **Applying behavioural level test generation to high-level design validation**
Gulbins, M.; Straube, B.;
European Design and Test Conference, 1996. ED&TC 96. Proceedings , 11-14 March 1996
Pages:613

[Abstract] [PDF Full-Text (96 KB)] IEEE CNF

---

16 **Rapid prototyping for communications design validation**
Courtoy, M.;
Northcon/96 , 4-6 Nov. 1996
Pages:162 - 167

[Abstract] [PDF Full-Text (740 KB)] IEEE CNF

---

17 **First test results of system level fault tolerant design validation thr laser fault injection**

Moreno, W.A.; Falquez, F.J.; Samson, J.R., Jr.; Smith, T.;
Computer Design: VLSI in Computers and Processors, 1997. ICCD '97. Proceedings., 1997 IEEE International Conference on , 12-15 Oct. 1997
Pages:544 - 548

[Abstract] [PDF Full-Text (596 KB)] IEEE CNF

---

18 **DSP Quant: design, validation, and applications of DSP hard real-ti benchmark**
Chunho Lee; Kirovski, D.; Hong, I.; Potkonjak, M.;
Acoustics, Speech, and Signal Processing, 1997. ICASSP-97., 1997 IEEE International Conference on , Volume: 1 , 21-24 April 1997
Pages:679 - 682 vol.1

[Abstract] [PDF Full-Text (308 KB)] IEEE CNF

---

19 **Design validation of the PBFA-Z vacuum insulator stack**
Shoup, R.W.; Long, F.; Martin, T.H.; Spielman, R.B.; Stygar, W.A.; Mostrom, Struve, K.W.; Ives, H.; Corcoran, P.; Smith, I.;
Pulsed Power Conference, 1997. Digest of Technical Papers. 1997 11th IEEE International , Volume: 2 , 29 June-2 July 1997
Pages:1608 - 1613 vol.2

[Abstract] [PDF Full-Text (420 KB)] IEEE CNF

---

20 **Fault tolerant design validation through laser fault injection [space based computing systems]**
Moreno, W.A.; Falquez, F.J.; Saini, N.;
Devices, Circuits and Systems, 1998. Proceedings of the 1998 Second IEEE International Caracas Conference on , 2-4 March 1998
Pages:132 - 137

[Abstract] [PDF Full-Text (528 KB)] IEEE CNF

---

21 **Design, Validation, And Application Of A System To Measure Cross Sectional Area In The Rat Achilles Tendon**
Love, C.L.; Korvick, D.L.; Lanctot, D.R.; Agrawal, C.M.; Athanasiou, K.A.;
Biomedical Engineering Conference, 1998. Proceedings of the 17th Southern , Feb. 1998
Pages:25 - 25

[Abstract] [PDF Full-Text (116 KB)] IEEE CNF

---

22 **Tutorial 3 High-level Design Validation And Test**
Dey, S.; Abraham, J.; Zorian, Y.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on , 8-12 Nov. 1998
Pages:3 - 3

[Abstract] [PDF Full-Text (92 KB)] IEEE CNF

---

23 **Native mode functional test generation for processors with applica to self test and design validation**

Jian Shen; Abraham, J.A.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:990 - 999

[Abstract] [PDF Full-Text (904 KB)] IEEE CNF

---

24 **A lifecycle approach to design validation is it necessary? Is it feasit**
Stoica, S.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:784 - 792

[Abstract] [PDF Full-Text (632 KB)] IEEE CNF

---

25 **Towards an automatic diagnosis for high-level design validation**
Khalil, M.; Le Traon, Y.; Robach, C.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:1010 - 1018

[Abstract] [PDF Full-Text (612 KB)] IEEE CNF

---

26 **Rapid system prototyping for real-time design validation**
Courtoy, M.;
Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Work: on , 3-5 June 1998
Pages:108 - 112

[Abstract] [PDF Full-Text (296 KB)] IEEE CNF

---

27 **Measuring the effectiveness of various design validation approache PowerPC™ microprocessor arrays**
Wang, L.-C.; Abadir, M.S.; Zeng, J.;
Design, Automation and Test in Europe, 1998., Proceedings , 23-26 Feb. 199{
Pages:273 - 277

[Abstract] [PDF Full-Text (196 KB)] IEEE CNF

---

28 **Design validation of .18 µm 1 GHz cache and register arrays**
Malone, D.;
Memory Technology, Design and Testing, 1999. Records of the 1999 IEEE International Workshop on , 9-10 Aug. 1999
Pages:54 - 60

[Abstract] [PDF Full-Text (104 KB)] IEEE CNF

---

29 **Component-based systems as an aid to design validation**
Henderson, P.; Walters, R.;
Automated Software Engineering, 1999. 14th IEEE International Conference o , 12-15 Oct. 1999
Pages:303 - 306

[Abstract] [PDF Full-Text (48 KB)] IEEE CNF

---

30 **System design validation using formal models**

Henderson, P.; Walters, R.;
Rapid System Prototyping, 1999. IEEE International Workshop on , 16-18 Jun 1999
Pages:10 - 14

[Abstract] [PDF Full-Text (56 KB)] **IEEE CNF**

---

31 **Design validation of .18 µm 1 GHz cache and register arrays**
Malone, D.; Bunce, P.; DellaPietro, J.; Davis, J.; Dawson, J.; Knips, T.; Plass, Pritzlaff, P.; Reyer, K.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Pages:295 - 298

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

---

32 **VHDL design validation by genetic manipulation techniques**
Stamenkovic, Z.; Dahmen, H.-Ch.; Glaeser, U.;
Microelectronics, 2000. Proceedings. 2000 22nd International Conference on , Volume: 2 , 14-17 May 2000
Pages:735 - 738 vol.2

[Abstract] [PDF Full-Text (156 KB)] **IEEE CNF**

---

33 **Proceedings IEEE International High-Level Design Validation and T Workshop (Cat. No.PR00786)**

High-Level Design Validation and Test Workshop, 2000. Proceedings. IEEE International , 8-10 Nov. 2000
[Abstract] [PDF Full-Text (176 KB)] **IEEE CNF**

---

34 **IC design validation using message sequence charts**
Vranken, H.; Garcia, T.G.; Mauw, S.; Feils, L.;
Euromicro Conference, 2000. Proceedings of the 26th , Volume: 1 , 5-7 Sept.

Pages:122 - 127 vol.1

[Abstract] [PDF Full-Text (412 KB)] **IEEE CNF**

---

35 **Guest editor's introduction to special section on high-level design validation and test**
Karri, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 , Issue: 3 , March 2001
Pages:353 - 354

[Abstract] [PDF Full-Text (12 KB)] **IEEE JNL**

---

36 **Design validation of embedded dependable systems**
Bondavalli, A.; Fantechi, A.; Latella, D.; Simoncini, L.;
Micro, IEEE , Volume: 21 , Issue: 5 , Sept.-Oct. 2001
Pages:52 - 62

[Abstract] [PDF Full-Text (128 KB)] IEEE JNL

---

37 **Efficient coverage analysis metric for HDL design validation**
Liu, C.-N.; Jou, J.-Y.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 148 , Issue: 1
2001
Pages:1 - 6

[Abstract] [PDF Full-Text (580 KB)] IEE JNL

---

38 **Sixth IEEE International High-Level Design Validation and Test Workshop**

High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEI
International , 7-9 Nov. 2001
[Abstract] [PDF Full-Text (154 KB)] IEEE CNF

---

39 **RTL design validation, DFT and test pattern generation for high def coverage**
Santos, M.B.; Gonqalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;
Test Workshop, IEEE European, 2001 , May 29 - Jun. 1, 2001
Pages:99 - 105

[Abstract] [PDF Full-Text (560 KB)] IEEE CNF

---

40 **An MOS transistor model for RF IC design valid in all regions of operation**
Enz, C.;
Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue
1 , Jan. 2002
Pages:342 - 359

[Abstract] [PDF Full-Text (590 KB)] IEEE JNL

---

41 **A new time model for the specification, design, validation and synt of embedded real-time systems**
Munzenberger, R.; Dorfel, M.; Slomka, F.; Hofmann, R.;
Design, Automation and Test in Europe Conference and Exhibition, 2002.
Proceedings , 4-8 March 2002
Pages:1095

[Abstract] [PDF Full-Text (177 KB)] IEEE CNF

---

42 **Proceedings Seventh IEEE International High-Level Design Validati and Test Workshop**

High-Level Design Validation and Test Workshop, 2002. Seventh IEEE
International , 27-29 Oct. 2002
[Abstract] [PDF Full-Text (295 KB)] IEEE CNF

---

43 **Eighth IEEE International High-Level Design Validation and Test Workshop**

High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
[Abstract] [PDF Full-Text (346 KB)] IEEE CNF

---

44 **The confluence of manufacturing test and design validation**
Harris, I.G.;
Test Conference, 2003. Proceedings. ITC 2003. International , Volume: 1 , Se 30-Oct. 2, 2003
Pages:1290 - 1290

[Abstract] [PDF Full-Text (192 KB)] IEEE CNF

---

45 **The confluence of manufacturing test and design validation**
Fummi, F.;
Test Conference, 2003. Proceedings. ITC 2003. International , Volume: 1 , Se 30-Oct. 2, 2003
Pages:1291 - 1291

[Abstract] [PDF Full-Text (271 KB)] IEEE CNF

---

46 **Design validation of ZCSP with SPIN**
Beaudenon, V.; Encrenaz, E.; Desbarbieux, J.-L.;
Application of Concurrency to System Design, 2003. Proceedings. Third International Conference on , 18-20 June 2003
Pages:102 - 110

[Abstract] [PDF Full-Text (284 KB)] IEEE CNF

---

47 **Automatic design validation framework for HDL descriptions via RT ATPG**
Liang Zhang; Hsiao, M.; Ghosh, I.;
Test Symposium, 2003. ATS 2003. 12th Asian , 16-19 Nov. 2003
Pages:148 - 153

[Abstract] [PDF Full-Text (273 KB)] IEEE CNF

---

48 **The confluence of manufacturing test and design validation**
Kwang-Ting Tim Cheng;
Test Conference, 2003. Proceedings. ITC 2003. International , Volume: 1 , Se 30-Oct. 2, 2003
Pages:1293 - 1293

[Abstract] [PDF Full-Text (218 KB)] IEEE CNF

---

49 **Call for Papers for Special Issue on Simulation-Based Design Valida**

Computers, IEEE Transactions on , Volume: 53 , Issue: 10 , Oct. 2004
Pages:1360 - 1360

[PDF Full-Text (31 KB)] IEEE JNL

---

50 **An ISO market settlement design validation approach using probabilistic market simulation study techniques**

Petrov, V.; Kumar, J.; Richter, C.;
ProbabilisticMethods Applied to Power Systems, 2004 International Conferenc
on , 12-16 Sept. 2004
Pages:338 - 342

[Abstract] [PDF Full-Text (651 KB)] **IEEE CNF**

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verif*)) <and> remov*
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---

1 **Cleanroom software engineering-plan your work and work your plar small increments**
Spangler, A.;
Potentials, IEEE , Volume: 15 , Issue: 4 , Oct.-Nov. 1996
Pages:29 - 32

[Abstract] [PDF Full-Text (1080 KB)] IEEE JNL

---

2 **Exploitation of Hierarchy in Analyses of Integrated Circuit Artwork**
Newell, M.E.; Fitzpatrick, D.T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 1 , Issue: 4 , October 1982
Pages:192 - 200

[Abstract] [PDF Full-Text (1288 KB)] IEEE JNL

---

3 **Formal verification of digital systems by automatic reduction of data paths**
Macii, E.; Plessier, B.; Somenzi, F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 10 , Oct. 1997
Pages:1136 - 1156

[Abstract] [PDF Full-Text (804 KB)] IEEE JNL

---

4 **Matching in the presence of don't cares and redundant sequential elements for sequential equivalence checking**
Rahim, S.; Rouzeyre, B.; Torres, L.; Rampon, J.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003

Pages:129 - 134

[Abstract] [PDF Full-Text (378 KB)] IEEE CNF

---

5 **Redundant functional faults reduction by saboteurs synthesis [logic verification]**
Fummi, F.; Marconcini, C.; Pravadelli, G.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
Pages:108 - 113

[Abstract] [PDF Full-Text (432 KB)] IEEE CNF

---

6 **General framework for removal of clock network pessimism**
Zejda, J.; Frain, P.;
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conferen on , 10-14 Nov. 2002
Pages:632 - 639

[Abstract] [PDF Full-Text (603 KB)] IEEE CNF

---

7 **Emulation-based design errors identification**
Castelnuovo, A.; Fin, A.; Fummi, F.; Sforza, F.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 1 IEEE International Symposium on , 6-8 Nov. 2002
Pages:365 - 371

[Abstract] [PDF Full-Text (895 KB)] IEEE CNF

---

8 **Design for verification at the register transfer level**
Ghosh, I.; Sekar, K.; Boppana, V.;
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asi South Pacific and the 15th International Conference on VLSI Design. Proceedi , 7-11 Jan. 2002
Pages:420 - 425

[Abstract] [PDF Full-Text (366 KB)] IEEE CNF

---

9 **Constraints specification at higher levels of abstraction**
Balarin, F.; Burch, J.; Lavagno, L.; Watanabe, Y.; Passerone, R.; Sangiovanni Vincentelli, A.;
High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IE International , 7-9 Nov. 2001
Pages:129 - 133

[Abstract] [PDF Full-Text (173 KB)] IEEE CNF

---

10 **Estimation of aperture response functions from measurements usir non-ideal detector**
Clinthorne, N.H.; Wrobel, M.C.; Ng, C.; Rogers, W.L.;
Nuclear Science Symposium and Medical Imaging Conference Record, 1995., IEEE , Volume: 2 , 21-28 Oct. 1995
Pages:958 - 962 vol.2

[Abstract] [PDF Full-Text (428 KB)] IEEE CNF

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((design <near/1> valid*)
<or> (design <near/1>
verif*)) and (remov* <near/5>
defect* <near/5> data)
```

Start Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search operators: <and> <or> <not> <in> More

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1 **Cleanroom software engineering-plan your work and work your plar small increments**
Spangler, A.;
Potentials, IEEE , Volume: 15 , Issue: 4 , Oct.-Nov. 1996
Pages:29 - 32

[Abstract] [PDF Full-Text (1080 KB)] **IEEE JNL**

---

2 **Emulation-based design errors identification**
Castelnuovo, A.; Fin, A.; Fummi, F.; Sforza, F.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 1
IEEE International Symposium on , 6-8 Nov. 2002
Pages:365 - 371

[Abstract] [PDF Full-Text (895 KB)] **IEEE CNF**

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1 **Functional test generation for full scan circuits**
Pomeranz, I.; Reddy, S.M.;
Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings , 27-30 March 2000
Pages:396 - 401

[Abstract] [PDF Full-Text (40 KB)] IEEE CNF

---

2 **Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159)**

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000
[Abstract] [PDF Full-Text (544 KB)] IEEE CNF

---

3 **RTL-based functional test generation for high defects coverage in di SOCs**
Santos, M.B.; Goncalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;
European Test Workshop, 2000. Proceedings. IEEE , 23-26 May 2000
Pages:99 - 104

[Abstract] [PDF Full-Text (508 KB)] IEEE CNF

---

4 **Proceedings 18th IEEE VLSI Test Symposium**

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000
[Abstract] [PDF Full-Text (728 KB)] IEEE CNF

---

5 **Validating fault tolerant designs using laser fault injection (LFI)**
Samson, J.R., Jr; Moreno, W.; Falquez, F.;
Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE

International Symposium on , 20-22 Oct. 1997
Pages:175 - 183

[Abstract] [PDF Full-Text (684 KB)] IEEE CNF

---

6 **A method for the evaluation of behavioral fault models**
Gaudette, E.; Moussa, M.; Harris, I.G.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
Pages:169 - 172

[Abstract] [PDF Full-Text (379 KB)] IEEE CNF

---

7 **Software-based self-test methodology for crosstalk faults in proces**
Xiaoliang Bai; Li Chen; Dey, S.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
Pages:11 - 16

[Abstract] [PDF Full-Text (524 KB)] IEEE CNF

---

8 **Proceedings International Test Conference 2002 (Cat. No.02CH3738**

Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002
[Abstract] [PDF Full-Text (545 KB)] IEEE CNF

---

9 **RTL design validation, DFT and test pattern generation for high defe coverage**
Santos, M.B.; Gonqalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;
Test Workshop, IEEE European, 2001 , May 29 - Jun. 1, 2001
Pages:99 - 105

[Abstract] [PDF Full-Text (560 KB)] IEEE CNF

---

10 **International Test Conference 1999. Proceedings (IEEE Cat. No.99CH37034)**

Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999
[Abstract] [PDF Full-Text (600 KB)] IEEE CNF

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11 **Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270)**

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
[Abstract] [PDF Full-Text (660 KB)] IEEE CNF

---

12 **I_{DDQ} testing and defect classes-a tutorial**
Soden, J.M.; Hawkins, C.F.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , May 1995
Pages:633 - 642

[Abstract] [PDF Full-Text (956 KB)] IEEE CNF

13 **A methodology for rapid prototyping of real-time image processing systems**

Kralijic, I.C.; Quenot, G.M.; Zavidovique, B.;

Rapid System Prototyping, 1995. Proceedings., Sixth IEEE International Work: on , 7-9 June 1995

Pages:97 - 103

[Abstract] [PDF Full-Text (692 KB)] IEEE CNF

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... **model-to-hardware correlation** at different points in the. process distribution. Other parameters of interest are voltage range ...
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[PDF] The I/O Power Supply Modeling For Pentium 4 Microprocessor Packaging
File Format: PDF/Adobe Acrobat - View as HTML
... 6. REFERENCES. [1] S. Chun, L. Smith, R. Anderson, M. Swaminathan, "**Model to**

hardware correlation for power distribution induced ...
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... **Daniel Coops**, 73, Cheshire Toft, Lancaster, Salford, Joiner, 3736, 69. John Coops, 43, Lancs Manchester, Manchester, Manchester, Merchant Traveller ...
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